REMARKS

Applicant is in receipt of the Office Action mailed September 30, 2003. Claims 5 and 27 have been amended to address the 35 U.S.C. 112, second paragraph, rejection of those claims. Claims 1, 7, and 19 have been amended to more clearly indicate the scope of the invention. Claims 2 and 8 have been cancelled. Thus, claims 1, 3-7, and 9-42 remain pending in the case. Further consideration of the present case is earnestly requested in light of the following remarks.

Section 102 Rejections

Claims 1-30 were rejected under 35 U.S.C. 102(e) as being anticipated by von der Wense (US 6598107, "von der Wense"). Applicant respectfully disagrees.

As the Examiner is surely aware, anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 221 USPQ 481, 485 (Fed. Cir. 1984). The identical invention must be shown in as complete detail as is contained in the claims. Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Currently amended claim 1 recites:

1. (currently amended) A system for interfacing a host computer to a Controller Area Network (CAN) bus, the system comprising:

a memory configured to store program code;

an embedded processor coupled to the memory, and configured to execute the program code;

bus interface logic coupled to the embedded processor, wherein the bus interface logic is operable to couple to an interconnecting bus, wherein the bus interface logic is adapted to interface with a device through the interconnecting bus;

CAN interface logic coupled to the embedded processor and adapted for interfacing with the CAN bus;

wherein the embedded processor is operable to execute the program code to perform a CAN event in response to said bus interface logic receiving a trigger signal on the interconnecting bus from the device; and

wherein, in response to receiving the trigger signal, the embedded processor is operable to perform the CAN event substantially synchronously with an event performed by the peripheral device.

The Office Action asserts that von der Wenser teaches all the features and limitations of claim 1, including CAN interface logic and the processor operable to execute the program code to perform a CAN event in response to the bus interface logic receiving a trigger signal on the interconnecting bus from the device, citing col. 5, lines 42-50. Applicant respectfully disagrees.

The cited passage describes independently clocked master and slave units coupled via a serial bus, where the master unit communicates a signal pattern for a predetermined period of time to the serial bus to set the bus to a definite state prior to initiating frame based communication between the units. As described elsewhere in von der Wenser, the slave unit may respond to the signal pattern by going to an alert state from standby mode, e.g., after the signal pattern has toggled, after which the frame based communication between the units may be performed.

This is in contrast to the system described in claim 1, where an embedded processor responds to a received trigger signal on an interconnecting bus from a device by executing program code to perform a CAN event, where the CAN event is substantially synchronous with an event performed by the device. Applicant notes that in the system described in claim 1, the interconnecting bus (between the device and the processor/bus interface logic) is distinct from the CAN bus, i.e., there are two different buses in the system, whereas in the system of von der Wenser, only one bus is used. Applicant also submits that it would be improper to interpret the slave unit going to an alert state as a CAN event, since the slave unit can only perform or generate an event *after* going into the alert state. Applicant also notes that nowhere does von der Wenser describe or even mention triggers.

Additionally, von der Wenser fails to teach or suggest *the CAN event and the device event being performed substantially in synchrony.* While the Office Action cited col. 5, lines 42-44 in asserting that von der Wenser discloses "the CAN event substantially synchronous with a peripheral device event", Applicant can find no mention of this feature in the cited passage, nor anywhere else in von der Wenser. Thus, Applicant submits that von der Wenser fails to teach all of the limitations and features of claim 1.

Thus, Applicant respectfully submits that claim 1, and claims dependent thereon, are patentably distinct over von der Wenser, and are thus allowable for at least the reasons provided above.

The Office Action further asserts that von der Wenser teaches all the features and limitations of claim 7, including a memory configured to store program code, citing col. 5, lines 8-31, an embedded processor configured to execute the program code, citing col. 5, lines 36-37, bus interface logic coupled to the embedded processor adapted to interface with a device, citing col. 4, lines 55-64, CAN interface logic, citing col. 5, lines 42-50, and wherein the bus interface logic is configured to assert a trigger signal on the interconnecting bus to the device in response to the embedded processor performing a CAN event, citing col. 5, lines 9-11. Applicant respectfully disagrees.

Currently amended claim 7 recites:

7. (currently amended) A system for interfacing a host computer to a Controller Area Network (CAN) bus, the system comprising:

a memory configured to store program code;

an embedded processor coupled to the memory, and configured to execute the program code;

bus interface logic coupled to the embedded processor, wherein the bus interface logic is operable to couple to an interconnecting bus, wherein the bus interface logic is adapted to interface with a device through the interconnecting bus;

CAN interface logic coupled to the embedded processor and adapted for interfacing with the CAN bus;

wherein the bus interface logic is configured to assert a trigger signal on the interconnecting bus to the device in response to the embedded processor performing a CAN event, wherein the trigger signal is useable to direct the device to perform an event substantially synchronously with the CAN event.

The arguments provided above in reference to claim 1 may be similarly applied to claim 7, but rather than the processor performing a CAN event in response to a trigger signal on the interconnecting bus (as in claim 1), the bus interface logic is configured to assert a trigger signal on the interconnecting bus in response to the processor performing a CAN event. As discussed above, the cited passages of von der Wenser describe a system with one bus, as opposed to the two buses, i.e., the CAN bus and the interconnecting bus, of claim 7. Applicant also notes that nowhere (in the cited passages or elsewhere) does von der Wenser teach or suggest a processor asserting a trigger signal on the interconnecting bus in response to a CAN event. Additionally, von der Wenser fails to teach or suggest *the trigger signal being useable to direct the device to perform an event substantially synchronously with the CAN event.* As noted above, while the Office Action cited col. 5, lines 42-44 in asserting that von der Wenser discloses this feature, Applicant can find no mention of this feature in the cited passage, nor anywhere else in the reference. Thus, Applicant submits that von der Wenser fails to teach all of the limitations and features of claim 7.

Thus, Applicant respectfully submits that claim 7, and claims dependent thereon, are patentably distinct over von der Wenser, and are thus allowable for at least the reasons provided above.

The Office Action further asserts that von der Wenser teaches all the features and limitations of claim 14, including receiving a trigger signal on the interconnecting bus from the device, and performing a CAN event in response..., citing col. 5, lines 42-50, and the CAN event *substantially synchronous with a peripheral device event*, citing col. 5, lines 42-44. Applicant respectfully disagrees.

Claim 14 recites:

14. A method for operating a Controller Area Network (CAN) interface, wherein the CAN interface and a peripheral device are both coupled to a host computer, wherein the CAN interface and the peripheral device are directly coupled through an interconnecting bus, the method comprising:

the CAN interface receiving a trigger from the peripheral device through an interconnecting bus; and

the CAN interface performing a CAN event in response to the trigger signal;

wherein, in response to receiving the trigger signal, the CAN interface performs the CAN event substantially synchronously with an event performed by the peripheral device.

As discussed above, von der Wenser does not teach or describe performing a CAN event in response to a trigger signal received from a peripheral device through an interconnecting bus, and specifically does not describe *performing the CAN event substantially synchronously with an event performed by the peripheral device in response to receiving the trigger signal.* Thus, Applicant submits that von der Wenser fails to teach all of the limitations and features of claim 14.

Thus, Applicant respectfully submits that claim 14, and claims dependent thereon, are patentably distinct over von der Wenser, and are thus allowable for at least the reasons provided above.

The Office Action further asserts that von der Wenser teaches all the features and limitations of claim 19, including the CAN interface performing a CAN event, the CAN interface transmitting a trigger signal to the peripheral device through the interconnecting bus in response to the CAN interface performing the CAN event, wherein the trigger signal is operable to direct the peripheral device to perform a peripheral event in response to the trigger signal, citing col. 5, lines 9-11. Applicant respectfully disagrees.

Currently amended claim 19 recites:

19. A method for operating a Controller Area Network (CAN) interface, wherein the CAN interface and a peripheral device are both coupled to a host computer,

wherein the CAN interface and the peripheral device are directly coupled through an interconnecting bus, the method comprising:

the CAN interface performing a CAN event;

the CAN interface transmitting a trigger signal to the peripheral device through the interconnecting bus in response to the CAN interface performing the CAN event;

wherein the trigger signal is operable to direct the peripheral device to perform a peripheral event substantially synchronously with the CAN event in response to the trigger signal.

The cited passage of von der Wenser merely states "According to the new ratio the period of the signal pattern is updated then." Applicant respectfully submits that nowhere (in the cited passages or elsewhere) does von der Wenser teach or suggest a CAN interface performing a CAN event, and the CAN interface transmitting a trigger signal to a peripheral device through an interconnecting bus in response to the CAN interface performing the CAN event, wherein the trigger signal is operable to direct the peripheral device to perform a peripheral event *substantially synchronously with the CAN event* in response to the trigger signal. Thus, Applicant submits that von der Wenser fails to teach all of the limitations and features of claim 19.

Thus, Applicant respectfully submits that claim 19, and claims dependent thereon, are patentably distinct over von der Wenser, and are thus allowable for at least the reasons provided above.

The Office Action further asserts that von der Wenser teaches all the elements and limitations of claim 24, including a peripheral device coupled to the host computer system, citing col. 5, lines 8-31, a CAN bus, citing col. 1, lines 32-33, one or more CAN devices, citing col. 1, lines 28-29, an interconnecting bus, citing col. 1, lines 15-21, and where the CAN interface device and the peripheral device are operable to communicate with each other using the interconnecting bus to synchronize measurement and/or control operations on the physical system. Applicant respectfully disagrees.

Claim 24 recites:

24. A system for performing a measurement on a physical system, the system comprising:

a host computer system;

a peripheral device coupled to the host computer system, wherein the peripheral device couples to the physical system;

a Controller Area Network (CAN) bus;

one or more CAN devices coupled to the CAN bus, wherein the one or more CAN devices couple to the physical system;

an interconnecting bus; and

a CAN interface device coupled to the host computer system, wherein the CAN interface device is directly coupled to the peripheral device through the interconnecting bus;

wherein the CAN interface device and the peripheral device are operable to communicate with each other using the interconnecting bus to synchronize measurement and/or control operations on the physical system.

Applicant notes that, as mentioned above, the system described by von der Wenser includes only one bus, e.g., a CAN bus, and specifically does not teach or suggest a peripheral device coupled to a host computer system and to a physical system (e.g., a unit under test), a CAN bus coupled to one or more CAN devices which further couple to the physical system, an interconnecting bus, and a CAN interface device coupled to the host computer system, where the CAN interface device is directly coupled to the peripheral device through the interconnecting bus, and where the CAN interface device and the peripheral device are operable to communicate with each other *using the interconnecting bus to synchronize measurement and/or control operations on the physical system*. Applicant notes that von der Wenser describes synchronizing various clocks once the units are in alert mode, but specifically does not teach the elements and their relationships as presented in claim 24. Thus, Applicant submits that von der Wenser fails to teach all of the limitations and features of claim 24.

Thus, Applicant respectfully submits that claim 24, and claims dependent thereon, are patentably distinct over von der Wenser, and are thus allowable for at least the reasons provided above.

Claims 2 and 8 were cancelled, and so the 102 rejection of these claims is moot. For at least the reasons provided above, Applicant respectfully submits that claims 1, 3-7, and 9-30 are patentably distinct over von der Wenser, and are thus allowable. Applicant respectfully requests removal of the 102 rejection of these claims.

Section 103 Rejections

Claims 1-42 were rejected under 35 U.S.C. 103(a) as being unpatentable over Rao (US 2003/0028701, "Rao") in view of von der Wense (US 6598107, "von der Wense"), and further in view of Pinto ("networked, intelligent I/O, the truly distributed control revolution", ISA Proceedings, December 1999, "Pinto"). Applicant respectfully disagrees.

As held by the U.S. Court of Appeals for the Federal Circuit in Ecolochem Inc. v. Southern California Edison Co., an obviousness claim that lacks evidence of a suggestion or motivation for one of skill in the art to combine prior art references to produce the claimed invention is defective as hindsight analysis.

In addition, the showing of a suggestion, teaching, or motivation to combine prior teachings "must be clear and particular . . .. Broad conclusory statements regarding the teaching of multiple references, standing alone, are not 'evidence'." *In re Dembiczak*, 175 F.3d 994, 50 USPQ2d 1614 (Fed. Cir. 1999). The art must fairly teach or suggest to one to make the specific combination as claimed. That one achieves an improved result by making such a combination is no more than hindsight without an initial suggestion to make the combination.

The Office Action asserts that Rao discloses a memory configured to store program code and an embedded processor configured to execute the program code, bus

interface logic coupled to the embedded processor, adapted to interface with a device, local I/O bus interface logic and the processor operable to execute the program code to perform an event in response to the bus interface logic receiving a trigger signal on the interconnecting bus from the device, citing paragraph 19, and figure items 100, 142, and 166. The Office Action further asserts that it would have been obvious to use the CAN bus disclosed by von der Wenser as the local I/O bus of Rao, as exemplified by Pinto, to produce the features and limitations of claim 1 (and the other independent claims). Applicant respectfully disagrees.

Rao teaches a system and method of monitoring events of an integrated circuit (IC) data processor, where the events are related to different bus activity, such as, for example, device acquisition and ownership time, and number of requests and grants on a given bus (Abstract), as well as bus idle and data cycles, and number of retries. (paragraph 18). While Rao does discuss synchronization of events between different clock domains (see paragraphs 36 and 37), Applicant notes that this synchronization is performed via "qualifier circuits...designed to provide a qualifier pulse signal to synchronize events occurring in the A and B clock domains with events occurring in the C clock domain", and where "Events in the C clock domain are generated based on a clock signal having a frequency greater than or equal to the clock signal frequencies in both the A and B clock domains."

This is in contrast to the system of claim 1, where "the embedded processor is operable to execute the program code to perform a CAN event in response to said bus interface logic receiving a trigger signal on the interconnecting bus from the device, and where, in response to receiving the trigger signal, the embedded processor is operable to perform the CAN event substantially synchronously with an event performed by the peripheral device." Thus, Applicant respectfully submits that Rao does not teach or suggest the features and limitations of claim 1.

Applicant further submits that even if Rao is combined with von der Wenser (as exemplified by Pinto), the combination does not teach or suggest the all the limitations and features of claim 1. Applicant again notes that, as stated above, the art must fairly teach or suggest to one to make the specific combination as claimed. That one achieves an improved result by making such a combination is no more than hindsight without an

initial suggestion to make the combination. Applicant notes that none of the cited references provide or even hint at a motivation to combine, and so Applicant further submits that citing these references in the 103 rejection of claim 1 was improper.

Similar arguments apply with equal force to the 103 rejection of claims 14, 19, 24, 31, and 37.

Additionally, regarding claims 14 and 19, the Office Action asserts that Rao discloses the local I/O interface receiving a trigger through an interconnecting bus and the local I/O interface receiving the trigger signal and performing an I/O event substantially synchronously, citing figure item 138. Applicant notes that figure item 138 is merely a bridge to allow communication between two different buses (figure items 112 and 118), and in no way illustrates the CAN interface performing the CAN event substantially synchronously with an event performed by the peripheral device in response to receiving the trigger signal. Thus, Applicant respectfully submits that neither Rao, von der Wenser, nor Pinto, either singly or together, teach or suggest the limitations of claims 14 and 19.

Regarding claim 24, the Office Action asserts that Rao teaches "wherein the interface device is directly coupled to the peripheral device operable to synchronize measurement and/or control operations, citing figure items 146 and 138. Applicant notes that figure item 146 is a DMA (direct memory access) channel, and is thus not an interface device coupled to the host computer system, as taught in the present application. Nor do von der Wenser or Pinto teach this feature. Thus, Applicant respectfully submits that neither Rao, von der Wenser, nor Pinto, either singly or together, teach or suggest the limitations of claim 24.

Regarding claim 31, the Office Action asserts that Rao teaches "determining one or more of the data frames which correlate in time with the peripheral event", citing paragraph 36. Applicant notes that nowhere in the cited passage does Rao teach, suggest, or even mention data frames, and only mentions timestamps in the context of monitoring events to determine event frequency information. Additionally, while Rao does describe timestamping events (with the timestamp counter of Figure 6), Rao specifically does not teach or suggest "determining one or more of the data frames which correlate in time with the peripheral event". Thus, Applicant respectfully submits that neither Rao, von

der Wenser, nor Pinto, either singly or together, teach or suggest the limitations of claim 31.

Finally, regarding claim 37, the Office Action asserts that Rao discloses "a peripheral device transferring data values", citing paragraph 17 and figure items 112 and 144, the peripheral device generating peripheral timestamps indicating times-of-transference of said data values, citing paragraph 37 and Figure 6, an interface performing a frame transfer, citing paragraph 17 and figure items 118 and 146, and a trigger signal [and?] a trigger timestamp generated and determining from the peripheral timestamps the one or more data values, citing paragraph 37. Applicant respectfully disagrees.

Applicant notes that per Rao, "The time stamp counter provides a time reference so that a user may determine the frequency of the occurrences counted by the event counters. The total monitoring time can also be tracked by software reading the time stamp counter." (paragraph 23) Applicant notes that the time stamp counter is located in the monitoring facility in the integrated circuit data processor (see Figure 1, and so the timestamps are not generated by a peripheral device, thus, the timestamps are not properly "peripheral timestamps" as represented in claim 37 of the present application. Applicant further notes that nowhere does Rao teach or describe "determining from the peripheral timestamps the one or more data values". Applicant submits that neither von der Wenser nor Pinto teach these features, as well.

Thus, Applicant respectfully submits that neither Rao, von der Wenser, nor Pinto, either singly or together, teach or suggest the limitations of claim 37.

Applicant thus respectfully submits that each of the independent claims 1, 7, 14, 19, 24, 31, and 37, and claims dependent thereon, are patentably distinct over the cited art, and are thus allowable. Claims 2 and 8 were cancelled, and so the 103 rejection of these claims is moot. Thus, Applicant respectfully requests that the section 103 rejection of claims 1, 3-7, and 9-42 be removed.

In a more general sense, Applicant respectively submits that the two primary references (von der Wenser and Rao) both relate to correlation/synchronization of clocks

in different devices. For example, the von der Wenser patent makes it clear in the Background section that the clocks refer to oscillators or RC circuits. Similarly, the Rao application refers to interfacing an integrated circuit (IC) to different "clock domains" (different oscillator frequencies). Thus, both of these references apply to synchronization of clocks, referred to as "timing synchronization", e.g., when timebases are shared, such as with RTSI/PXI buses.

In contrast, in the present application, signals (e.g., RTSI signals) are used for stimulus/response behaviors, e.g., triggers and events, not clock synchronization. The stimulus/response behaviors fall into two general categories: A) when a trigger (e.g., a RTSI trigger signal) is received (stimulus), perform an action (e.g., a CAN event) (response), and B) when an event (a CAN event) occurs (stimulus), assert a trigger (e.g., a RTSI trigger) (response), each of which may be referred to as "trigger synchronization".

Thus, in summary, the systems described in the cited references relate to Timing, whereas the present application primarily relates to Triggering, and so Applicant submits that the cited references teach away from the present application.

Applicant also asserts that numerous ones of the dependent claims recited further distinctions over the cited art. However, since the independent claims have been shown to be patentably distinct, a further discussion of the dependent claims is not necessary at this time.

Thus, for at least the reasons provided above, Applicant respectfully submits that claims 1, 3-7, and 9-42 are patentably distinct over the cited art, and are thus allowable.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 50-1505/5150-22400/JCH.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

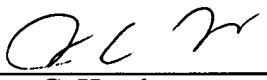
☐ Request for Approval of Drawing Changes

☐ Notice of Change of Address

☐ Check in the amount of $ for fees ( ).

☐ Other:

Respectfully submitted,



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